

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination ALON ET AL.	
		Examiner Naum B. Levin	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Siomacco et al., "Parametric modeling of integrated circuit interconnections", Circuits and Systems II: Analog and Digital Signal Processing, IEEE Volume 39, Issue 6, June 1992 Page(s):377 – 382.
	V	Un, M. et al., "Calculation of delay and rise times for uniformly distributed RLC line". Electrotechnical Conference, 1998. MELECON 98., 9th Mediterranean, Volume 1, 18-20 May 1998 Page(s):604 - 607.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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